[0015] Yet another embodiment relates to a method of providing redundancy in a memory structure. In this embodiment, the method comprises shifting out a first predecoder block; and shifting in a second predecoder block. It is further contemplated that shifting predecoded lines and shifting circuitry may be coupled to the first and second predecoder blocks.

[0016] Other aspects, advantages and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawing, wherein like numerals refer to like parts.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0017] FIG. **1** illustrates a block diagram of an exemplary SRAM module;

[0018] FIG. **2** illustrates a block diagram of a SRAM memory core divided into banks;

[0019] FIGS. **3**A and **3**B illustrate SRAM modules including a block structure or subsystem in accordance with one embodiment of the present invention;

[0020] FIG. **4** illustrates a dimensional block array or subsystem used in a SRAM module in accordance with one embodiment of the present invention;

[0021] FIG. **5** illustrates a cell array comprising a plurality of memory cells in accordance with one embodiment of the present invention;

[0022] FIG. **6**A illustrates a memory cell used in accordance with one embodiment of the present invention;

[0023] FIG. **6**B illustrates back-to-back inventors representing the memory cell of FIG. **6**A in accordance with one embodiment of the present invention;

[0024] FIG. **7** illustrates a SRAM module similar to that illustrated FIGS. **3**A and **3**B in accordance with one embodiment of the present invention;

[0025] FIG. **8** illustrates a local decoder in accordance with one embodiment of the present invention;

[0026] FIG. **9** illustrates a circuit diagram of a local decoder similar to that illustrated in FIG. **8** in accordance with one embodiment of the present invention;

[0027] FIG. **10** illustrates a block diagram of the local sense amps and 4:1 muxing in accordance with one embodiment of the present invention;

[0028] FIG. **11** illustrates a block diagram of the local sense amps and global sense amps in accordance with one embodiment of the present invention;

[0029] FIG. **12**A illustrates a schematic representation of the local sense amps and global sense amps in accordance with one embodiment of the present invention;

[0030] FIG. **12**B illustrates a circuit diagram of an embodiment of a local sense amp (similar to the local sense amp of FIG. **12**A) in accordance with one embodiment of the present invention;

[0031] FIG. **12**C illustrates a schematic representation of the amplifier core similar to the amplifier core illustrated in FIG. **12**B;

[0032] FIG. **13** illustrates a block diagram of another embodiment of the local sense amps and global sense amps in accordance with one embodiment of the present invention;

[0033] FIG. **14** illustrates a circuit diagram including a transmission gate of the 4:1 mux similar to that illustrated in FIGS. **10** and **12** in accordance with one embodiment of the present invention;

[0034] FIG. **15** illustrates transmission gates of the 2:1 mux coupled to the inverters of a local sense amp in accordance with one embodiment of the present invention;

[0035] FIG. **16** illustrates the precharge and equalizing portions and transmission gates of the 2:1 mux coupled to the inverters of a local sense amp in accordance with one embodiment of the present invention;

[0036] FIG. **17** illustrates a circuit diagram of the local sense amp in accordance with one embodiment of the present invention;

[0037] FIG. **18** illustrates a block diagram of a local controller in accordance with one embodiment of the present invention;

[0038] FIG. **19** illustrates a circuit diagram of the local controller in accordance one embodiment of the present invention;

[0039] FIG. **20** illustrates the timing for a READ cycle using a SRAM memory module in accordance with one embodiment of the present invention;

[0040] FIG. **21** illustrates the timing for a WRITE cycle using a SRAM memory module in accordance with one embodiment of the present invention;

[0041] FIG. **22**A illustrates a block diagram of local sense amp having 4:1 local muxing and precharging incorporated therein in accordance with one embodiment of the present invention;

[0042] FIG. **22**B illustrates one example of 16:1 muxing (including 4:1 global muxing and 4:1 local muxing) in accordance with one embodiment of the present invention;

[0043] FIG. **22**C illustrates one example of 32:1 muxing (including 8:1 global muxing and 4:1 local muxing) in accordance with one embodiment of the present invention;

[0044] FIG. **23** illustrates a local sense amp used with a cluster circuit in accordance with one embodiment of the present invention;

[0045] FIG. **24** illustrates a block diagram of one example of a memory module or architecture using predecoding blocks;

[0046] FIG. **25** illustrates a block diagram of another example of a memory module using predecoding blocks similar to that illustrated in FIG. **24**

[0047] FIG. **26**A illustrates a high-level overview of a memory module with predecoding and x- and y-Spill areas;

[0048] FIG. **26**B illustrates a high-level overview of a memory module with global and local predecoders;